REMARKS

Before this amendment, claim 1-18 were pending in the application. Applicants have cancelled claims 2 and 11-18, have amended claims 1 and 3-10 and have added new claims 19-23. Accordingly, claims 1, 3-10 and 19-23 are now pending in the present application.

Applicants respectfully submit that the claims as presented are allowable. The Examiner indicated that claim 4, 8, and 9 would be allowable if rewritten to overcome the 112 rejections and objections and to include all limitations of the base claim and any intervening claims. New claim 19 is a rewritten version of claim 4 in and claim 21 is a rewritten version of claim 8. Applicants respectfully submit that these claims meet the requirements of 35 U.S.C. § 112, second paragraph.

The Examiner rejected claim 1 under 35 U.S.C. § 102(b) as being anticipated by Takenaka et al. (US 5,449,299) ("Takenaka"). As amended, claim 1 recites that the first circuit comprises "a multiplexer (M1) configured to produce B= B_N on a first iteration and B= B_i on subsequent iterations where $B_N = (M - \alpha_N 2^N)$ and $B_i = (M' - \alpha_i 2^i)$ and where i is an iteration counter starting with N and counting down". Applicants respectfully submit that this feature is not shown in Takenaka. In rejecting claim 2, the Examiner cited to Figure 2 of Takenaka for support that this limitation was shown. After careful examination of Figure 2, however, it is clear that Takenaka does not show a multiplexer that is configured to pass $B_N = (M - \alpha_N 2^N)$ to the second circuit on a first iteration and pass $B_i = (M' - \alpha_i 2^i)$ on all subsequent iterations. No multiplexer is shown in Figure 2 of Takenaka. Takenaka discusses using adders and looping to perform a calculation. Nowhere in Takenaka is there a discussion to use multiplexers. Applicants respectfully submit that all of the limitations of claim 1 are not shown in Takenaka and that this claim is allowable over the art cited.

Regarding claims 3-9, these claims depend from claim 1 which applicants submit is allowable. Accordingly, claims 3-9 are at least allowable as depending from an allowable base claim.

The Examiner rejected claim 10 under 35 U.S.C. § 102(b) as being anticipated by Takenaka. Applicants respectfully submit that Takenaka does not show all of the limitations of

claim 10 and that claim 10 is allowable. Claim 10 recites a deinterleaver comprising a demultiplexer connected to a multiplexer through a circuit that is configured to calculate A modulo J. Takenaka discusses a method for encryption and does not discuss deinterleavers. Further, Takenaka does not show a demultiplexer connected to a multiplexer through a circuit. Accordingly, applicants respectfully submit that Takenaka does not show all of the limitations of claim 10 and that this claim is allowable.

Further, applicants respectfully submit that claims 1, 3-9 as amended comply with 35 U.S.C. § 112 and the Examiner's rejections and objections have been overcome.

REQUEST FOR ALLOWANCE

In view of the foregoing, Applicant submits that all pending claims in the application are patentable. Accordingly, reconsideration and allowance of this application are earnestly solicited. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below.

Dated: 1/10/05

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